# M.Tech (VLSI & Embedded Systems)

**Semester I**

| Code | Course Name | L–T-P Credits |
|---|---|---|
| EC 501 | Analog and Digital CMOS IC Design | 3-0-0 6 |
| EC 502 | Embedded System Design | 3-0-0 6 |
| EC 503 | Semiconductor Device Modeling | 3-0-0 6 |
| EC 5xx | Elective I | 3-0-0 6 |
| EC 5xx | Elective II | 3-0-0 6 |
| EC 511 | VLSI & Embedded Systems Lab I | 0-0-3 3 |
| | | 15-0-3 33 |

**Semester II**

| Code | Course Name | L-T-P Credits |
|---|---|---|
| EC 504 | Real Time Operating Systems | 3-0-0 6 |
| EC 505 | Embedded Signal Processing | 3-0-0 6 |
| EC 506 | VLSI DSP | 3-0-0 6 |
| EC 5xx | Elective III | 3-0-0 6 |
| EC 512 | VLSI & Embedded Systems Lab II | 0-0-3 3 |
| | | 15-0-3 27 |

**Semester III**

| Code | Course Name | L-T-P Credits |
|---|---|---|
| EC 611 | Thesis -I | 0-0-24 24 |

**Semester IV**

| Code | Course Name | L-T-P Credits |
|---|---|---|
| EC 612 | Thesis -II | 0-0-24 24 |

Total Credit = 108

**Departmental Electives**

| | | |
|---|---|---|
| EC521 | Wireless & Mobile Communication | 3-0-0-6 |
| EC522 | Fibre Optics Communication | 3-0-0-6 |
| EC523 | Modern Radio Communication | 3-0-0-6 |
| EC524 | Digital TV Engineering | 3-0-0-6 |
| EC525 | Low Power VLSI | 3-0-0-6 |
| EC526 | Radar Engineering | 3-0-0-6 |
| EC527 | FPGA Design | 3-0-0-6 |
| EC528 | Design of Digital System | 3-0-0-6 |
| EC529 | Soft Computing Techniques | 3-0-0-6 |
| EC530 | Microcontroller for Embedded System | 3-0-0-6 |
| EC531 | Embedded Computing | 3-0-0-6 |
| EC532 | Hardware Software Codesign | 3-0-0-6 |
| EC533 | Embedded Networking | 3-0-0-6 |
| EC534 | CPLD & FPGA Architecture | 3-0-0-6 |
| EC 535 | Semiconductor IC Technology | 3-0-0 6 |
| EC 536 | VLSI System Design | 3-0-0 6 |
| EC 537 | Linear Algebra and Optimization | 3-0-0 6 |
| EC 538 | Signal Processing Algorithms and Architectures | 3-0-0 6 |
| EC 539 | Optimal and Adaptive Signal Processing | 3-0-0 6 |
| EC 540 | Detection and Estimation Theory | 3-0-0 6 |
| EC 541 | ASIC Design and Modeling | 3-0-0 6 |
| EC 542 | Machine Intelligence | 3-0-0 6 |
| EC 543 | Reconfigurable Computing | 3-0-0 6 |
| EC 544 | Memory Technologies | 3-0-0 6 |
| EC 545 | VLSI EDA Tools | 3-0-0 6 |
| EC 546 | Fault Tolerant System Design | 3-0-0 6 |
| EC 547 | Biomedical Signals and Systems | 3-0-0 6 |
| EC 548 | Advanced Digital System Design | 3-0-0 6 |
| EC 549 | Embedded Automotive Systems | 3-0-0 6 |
| EC 550 | System-on-Chip (SoC) | 3-0-0 6 |
| EC 551 | Software Defined Radio | 3-0-0 6 |

| | | |
|---|---|---|
| EC552 | Smart Antenna | 3-0-0-6 |
| EC553 | Filters Design | 3-0-0-6 |

**EC501 Analog & Digital CMOD IC Design 3-0-0-6**

MOS Switch, MOS Diode/ Active Resistor, Current Sinks & Sources, Current Mirror, Current & Voltage Reference, Band gap References. Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifier Architectures. Buffered Opamp, High Speed/Frequency Opamps, Differential Output Opamps, Micro power Op amps, Low Noise Opamp. Low Voltage Opamp, Macro models for Opamps. Sequential Ckts. Design of FSM, Moore & Mealy machines, Metastability, Solutions to metastability, Synchronization methods, VHDL codes for complex sequential machines, Hazards, Types of hazards, Method to eliminate hazards, case studies. CMOS parasitic, Technology scaling, Lambda parameter, Design calculations for different logic ckts, Calculations for Area on chip, Power dissipation, PDP, Transmission gate, Domino logic, NORA logic, CMOS layout techniques, Transient response, Advance trends of elements & Alloys for ultra fast logic ckts.

## Texts :


1. J.M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits- A Design Perspective, 2nd ed., PHI, 2003
2. N.H.E. Weste and K. Eshraghian, Principles of CMOS VLSI Design – a System Perspective, 2nd ed., Pearson Education Asia, 2002
3. S.M. Kang and Y. Leblevici, CMOS Digital Integrated Circuits Analysis and Design, 3rd ed., McGraw Hill, 2003
4. J. P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & Sons (Asia) Pte Ltd, 2002
5. R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, IEEE Press, 1997.
6. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill 2001
7. P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd edition, Oxford University Press, 1997
8. B. Razavi, RF Microelectronics, Prentice-Hall, 1998.
9. P. R. Gray and R. G. Meyer, Analysis and design of Analog Integrated circuits 4th Edition, Wiley Student Edition, 2001.
10. D. A. Johns and K. Martin, Analog Integrated Circuit Design, Wiley Student Edition, 2002.


**EC 502 Embedded System Design 3-0-0 6**

Digital Systems and Embedded Systems, Design Methodology, Design Metrics, Specialties, Concepts & types of Memory, Cache Memory, Cache mapping techniques, replacement policies, Cache wire Techniques, Cache Impact on system Performance, Integrated Circuits Technologies- Full custom/VLSI, Logic Families, ASICs , PLDs, PALs, CPLDs , FPGA, Packaging and Circuit Boards, Interconnection and Signal Integrity , Differential Signaling. General Purpose Processor, System On chip, Embedded Computer Organization, ARM 7/ARM 9 architecture, ARM Microcontrollers and Processor Cores, Instructions and Data handling, interfacing with Memory, Interrupts, Timers, ARM Bus. I/O Devices, Controllers, Simple & Autonomous I/O Controllers, Parallel, Multiplexed, Tristate, and Open-Drain Buses, Bus Protocols, Serial Transmission Techniques & Standards, Wireless protocols, CAN & advanced Buses. Design Methodology, Design Flow, Architecture Exploration, Functional Design, Functional Verification, Synthesis, Physical Design, Design Optimization, Area Optimization, Timing Optimization, Power Optimization, Design for Test , Fault Models and Fault Simulation, Scan Design and Boundary Scan, Built-In Self Test (BIST), Nontechnical Issues.

**Texts/References:**


1. Digital Design: An Embedded Systems Approach Using Verilog, Peter J. Ashenden ELSEVIER, Morgan Kaufmann Publication, 2008.
2. Data books of ARM7/ARM9 J. Staunstrup and W. Wolf, editors, Hardware/Software Co- Design: Principles and Practice, Kluwer Academic Publishers, 1997.
3. G. DeMicheli, R. Ernst, and W. Wolf, editors, Readings in Hardware/Software Co-Design, Academic Press, 2002.


**EC 503 Semiconductor Device Modeling 3-0-0 6**

p-n Junctions: equilibrium conditions, forward and reverse-biased junctions, reverse-bias breakdown, transient and a-c conditions, recombination and generation in the transition, semiconductor heterojunctions, Metal-semiconductor junctions: Schottky barriers, rectifying and Ohmic contacts, Bipolar junction transistors: minority carrier distribution and terminal currents, generalized biasing, switching, secondary effects, frequency limitations of transistors, heterojunction bipolar transistors, Field-Effect Transistors: JFETcurrent- voltage characteristics, effects in real devices, high-frequency and high-speed issues, Metal Insulator Semiconductor

FET, MOSFETbasic operation and fabrication; ideal MOS capacitor; effects of real surfaces; threshold voltages; output and transfer characteristics of MOSFET, short channel and Narrow width effects, MOSFET scaling, Optoelectronics Devices: Light emitting diodes, Lasers, Photoconductors, Junction Photodiodes, Avalanche Photodiodes, Solar Cells, SPICE Models for Semiconductor Devices: MOSFET Level 1, Level 2 and level 3 model, Model parameters; SPICE models of p-n diode and BJT.

**Textss:**


1. B. G. Streetman and S. Banerjee, *Solid State Electronic Devices*, 6th Edition, PHI Private Limited, 2011.
2. P. Bhattacharya, *Semiconductor Optoelectronics Devices*, 2nd Edition, PHI, 2009.
3. G. Massobrio and P. Antognetti, *Semiconductor Device Modeling withSPICE*, 2nd Edition, TMH, 2010.
4. C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Pearson Education, 2010.
5. R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 3rd Edition, Wiley India, 2009.
6. S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd Edition, Wiley India, 2010.
7. Y. Tsividis, *Operation and Modeling of the MOS transistor*, 2nd Edition, TMH, 1999.
8. S. A. Neamen and D. Biswas, *Semiconductor Physics and Devices*, 4th Edition, TMH, 2012.


**EC5xx Elective I 3-0-0-6**

**EC5xx Elective II**

**EC511 VLSI & Embedded System Lab I 0-0-3-3**

**EC 504 Real Time Operating Systems 3-0-0 6**

Software Architectures, Software Developments Tools, Programming Concepts, Embedded Programming in C and C++, Queues, Stacks, Optimization of Memory needs, Program Modeling Concepts, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance, Operating System Concepts, Processes, Deadlocks, Memory Management, Input /Output, Files, Security, the Shell, Recycling of Concepts. Operating system structure Monolithic Systems: Layered Systems, Virtual Machines, Exo-kernels, Client-Server Model,Real Time Operating Systems (µC/OS):Real-Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization, Memory Management, and Porting µCos-II. Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes and Filters, File Protections, Shell Programming, System Programming, RT Linux Modules, POSIX Threads, Mutex Management, Semaphore Management.

**Texts:**


1. µC/OS-II, The real time Kernel, Jean J. Labrossy, Lawrence: R & D Publications, 2000.
2. Embedded Real Time Systems: Concepts, Design & Programming, Dr.K.V.K.K. Prasad, Dreamtech Publication, 2007.
3. An Embedded Software Primer, David E. Simon, Pearson Education Publication, 2005.
4. Modern Operating Systems, Second Edition, Andrew S. Tanenbaum, Prentice Hall Publication, 2001.
5. Embedded Systems Architecture, Programming and design, Raj Kamal, Tata MCgraw-Hill Publication, 1999.


**EC505 Embedded Signal Processing 3-0-0 6**

Digital Signal Processing Overview, Convolution, Correlation, Digital filters, DFT, STFT, DCT, wavelets and filter banks, FFT algorithms and Implementation, Representations of the DSP algorithms, Block diagrams, Signal flow graph, Data-flow graph, Dependence graph, iteration bounds, Pipelining and Parallel processing of FIR filters, Algorithm transformation: Retiming , Folding, Unfolding, Algorithmic strength reduction in Filters and Transforms, Parallel FIR filters, Fast FIR algorithms, Discrete cosine transform and Inverse DCT, Parallel processing for IIR filters, Pipelined adaptive digital filters. Introduction to Digital signal processing systems, MAC, Barrel shifter, ALU, Multipliers, Dividers, DSP processor architecture, Software developments, Selections of DSP processors, real time implementation considerations, Hardware interfacing, DSP processor architectures: TMS 320C54XX, TMS 320C67XX, Blackfin processor: Architecture overview, memory management, I/O management, On chip resources, programming considerations, Real time implementations, Applications of DSP systems: FIR filters, IIR filters, DTMF generation and detection, FFT algorithms, wavelet algorithms, Adaptive algorithms: system identification, inverse modeling, noise cancellation, prediction.

**Texts:**


1. Sen M. Kuo and Woon-Seng Gan, " Digital Signal Procesors, architectures, implementations, and applications", Prentice-Hall, 1999.
2. V. Madisetti, " The Digital Signal Processing Handbook", IEEE press, 2000

3. K. K. Parhi, “VLSI Digital Signal Processing Systems- Design and Implementation”, John Wiley & Sons, Inc, 2008.
4. Sanjit K. Mitra, “ Digital Signal Processing: A Computer based approach”, McCraw Hill, 1998.
5. Lawrence R. Rabiner and Bernard Gold, “Theory and application of Digital signal Processing”, Prentice-Hall of India, 2006.

**EC506 VLSI DSP 3-0-0 6**

Introduction to DSP systems: Representation of DSP algorithms; Iteration Bound: Definition, Examples, Algorithms for computing Iteration bound; Pipelining and Parallel Processing: Definitions, Pipelining and parallel processing of FIR filters, Pipelining and parallel processing for low power; Retiming: Definitions and Properties, Solving system of Inequalities, Retiming techniques; Unfolding: Definition, An algorithm for unfolding, Applications of unfolding; Folding: Definition, Folding transformations, Register minimization techniques, Register minimization in folded architectures; Systolic Architecture Design: Introduction, Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Matrix-Matrix multiplication and 2D systolic array design; CORDIC based Implementations: Architecture, Implementation of FIR filter and FFT algorithm; Bit-Level arithmetic architectures: Parallel multipliers, Bit-serial multipliers, Bit-Serial FIR filter design and Implementation; Redundant arithmetic: Redundant number representation, Carry-free radix-2 addition and subtraction, radix-2 hybrid redundant multiplication architectures; Low-power design: Theoretical background, Scaling versus power consumption, Power analysis, Power reduction techniques, Power estimation approaches.

**Texts / References:**

1. U. Meyer-Baese, DSP with FPGA, Springer, 2004.
2. K. K. Parhi, VLSI DSP Systems, Wiley, 2003.
3. R.G. Lyons, Understanding Digital Signal Processing, Pearson Education, 2004.

**EC5xx Elective II 0-0-3-6**

**EC 513 VLSI & Embedded Sytems Lab II 0-0-3 3**

The faculty associate with instruction of these subjects shall assign laboratory practices to the students, minimum three per course.

The laboratory practices shall encompass implementation/ deployment of the course work in terms of the hardware setup, algorithm development and programming assignment. The student shall submit a document as a bonafide record of such assignment in the hard/soft copy format to the concerned faculty for further evaluation.

**Texts / References:**

1. M. H. Rashid, *Introduction to PSpice Using OrCAD for Circuits and Electronics*, 3rd Edition, Prentice-Hall India, 2006.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill, 2001.
3. B. Razavi, *RF Microelectronics*, Prentice-Hall, 1998.
4. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd Edition, Oxford University Press, 1997.
5. D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, Wiley Student Edition, 2002.
6. P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th Edition, Wiley Student Edition, 2001.
7. Mentor Graphics CAD software manuals.

**EC521 Wireless & Mobile Communication 3-0-0-6**

Cellular concepts, frequency reuse, co channel interference, Cell splitting. Radio propagation characteristics; models for path loss, shadowing and multipath fading (delay spread, coherence bandwidth coherence time. Doppler spread). Jakes’ channel model. Digital modulation for mobile radio; analysis under fading channels; diversity techniques and Rake demodulator. Introduction to spread spectrum communication. Multiple access techniques used in mobile wireless communications: FDMA/TDMA, CDMA. The cellular concept: Frequency reuse; the basic theory of hexagonal cell layout; spectrum efficiency. FDM/TDM Cellular systems; channel allocation schemes. Handover analysis. Cellular CDMA; soft capacity. Erring capacity comparison of FDM/TDM systems and cellular CDMA. Discussion of GSM standards; signaling and call control; mobility management; location tracing. Wireless data networking; packet error modeling on fading channels, performance analysis of link and transport layer protocols over wireless channels; mobile data networking (mobile IP); wireless data in GSM, IS-95, and GPRS.

TEXTS:

1. Jochen Schiller, “Mobile Communications”, Second Edition, Pearson Education, 2003.
2. William Stallings, “Wireless Communications and Networks”, Pearson Education, 2002.

REFERENCES:
1. Kaveh Pahlavan, Prasanth Krishnamoorthy, “Principles of Wireless Networks”, First Edition, Pearson Education, 2003.
2. Uwe Hansmann, Lothar Merk, Martin S. Nicklons and Thomas Stober, “Principles of Mobile Computing”, Springer, 2003.
3. C.K.Toh, “AdHoc Mobile Wireless Networks”, First Edition, Pearson Education, 2002.

EC522 **FIBRE OPTICS COMMUNICATION** 3-0-0-6

Overview of Optical Communications, Optical Fibers, Signal Degradation, International standards, Review of Optical Sources, Review of Photo detectors, structures for InGaAs APDs, Temperature effect on avalanche gain, Optical receiver, Introduction to optical amplifiers (EDFA), Overview of WDM, Passive optical couplers, Isolators and Circulators.

TEXTS:
1. G.Keiser, Optical Fiber Communications, TMH, 4th Edition, 2008.
2. J. Gowar, Optical Communication Systems, PHI, 2nd Edition, 1993.

EC523 **MODERN RADIO COMMUNICATIONS** 3-0-0-6

Elements of a Communication Systems, FM Modulators, FET Phase Modulator, Foster-Seeley FM Discriminator, Ratio Detector, AM Transmitter, FM Transmitter, SSB Transmitter, TRF Radio Receiver, Super heterodyne Receiver, Image Frequency, AGC, SSB Transceiver, Special Features in Communication Receiver, Digital Radio, Television Broadcasting, TV Channels, TV Scanning, Indian TV Standards, composite video Signal, Functional blocks and operational aspects of each block of TV transmitter and receiver, CCD cameras, color TV display systems, Digital TV technology, HDTV systems.

TEXTS:
1. Louis E Frenzil, Communication Electronics: Principles and Applications, 3rd Edition, MGH, 2001.
2. George Kennedy and Bernard Davis, Electronic Communication Systems, TMH, 4th Edition, 2000.
3. BernardGrob, Basic Television and Video Systems, 6th Edition, MGH, Singapore, 2000.

EC524 **DIGITAL TV ENGINEERING** 3-0-0-6

Introduction, Digital Television Transmission standards, Performance objectives, Channel coding and modulation, Transmitters, Radio frequency systems, transmission lines, Transmitting antennas, radio wave propagation, Test and measurement.

TEXTS:
1. Modern Television Practice, Principles, Technology and Servicing, R.R. Gulati, 2nd Edition, New Age International Publishers, 2002.
2. Gerald W. Collins, Fundamentals of Digital Television Transmission, John Wiley, 2001.

EC525 **LOW POWER VLSI** 3-0-0-6

Low power CMOS VLSI design: Introduction, sources of power dissipation, designing for low power, physics of power dissipation in CMOS FET devices, Power estimation, synthesis for low power, Design and test of low-voltage CMOS circuits, Low power static RAM architectures, Low energy computing using energy recovery techniques. Software design for low power.

TEXTS:
1. Kaushik Roy, Sharat C Prasad, Low Power CMOS VLSI Circuit Design, Wiley Student Edition, 2009.
2. Jan M Rabaey, Digital Integrated Circuits, 2nd Edition, Pearson Education, 2003.

EC526 **RADAR ENGINNERING** 3-0-0-6

Radar and Radar Equation, Doppler Effect, CW Radar, FM - CW radar, altimeter, Multiple Frequency Radar, Pulse Radar, Pulse Doppler Radar, Tracking Radar, RADAR System Design, Matched Filter, Detector Characteristics, Phased Arrays, Advantages and Limitations Navigational Aids.

TEXTS:
1. M.I. Skolnik, Introduction Radar Systems, McGraw Hill Book Co., Fourth Edition, 2001.
2. G.S.N. Raju, Radar Engineering and Fundamentals and Navigational Aids, I.K. International, 2008
3. Simon Kingsley and Shaun Quegan, Understanding Radar Systems, SciTech Publishing, 1999.

EC527 **FPGA DESIGN** 3-0-0-6

Architecture vs organization, Design styles, Implementation styles, Design Examples using programmable logic devices, Design of Universal block. Design of memory, Floating point multiplier, Barrel shifter, Special purpose

Processors - Xilinx Vertex and Spartan - II; Altera FLEX 10k and other architectures. Design of parameterized library cells, Implementation and Testing- Xilinx,Actel and Altera FPGA based systems. Design - Case study.
TEXTS:
1. John V.Old Field, Richrad C.Dorf, Field Programmable Gate Arrays, John Wiley1995.
2. Michel John Sebastian Smith: Application Specific Integrated Circuits, Pearson, 1997.

EE528 **DESIGN OF DIGITAL SYSTEMS** 3-0-0-6
Principles of Sequential logic design: Concept of FSM - Metastability, State machine structures: Moore machine - Mealy machine, Analysis of state machine with D and J-K Flip-flops, Clocked synchronous state machine design, Designing state machine using state diagrams, State machine synthesis using transition list, Clock skew, Overview of PLDs, CPLDs and FPGAs, RT level combinational circuit, Regular sequential circuit, Design examples with VHDL.
TEXTS:
1. J. F. Wakerly: Digital Design-Principles and Practices, 4th Edition, Pearson, 2008.
2. Pong P. Chu: FPGA Prototyping by VHDL Examples: Xilinx Spartan-3 Version, 1st Edition, Wiley-Interscience, 2008.

**EC529 SOFT COMPUTING TECHNIQUES 3-0-0-6**
Basics of Fuzzy Sets: Fuzzy Relations – Fuzzy logic and approximate reasoning – Design Methodology of Fuzzy Control Systems – Basic structure and operation of fuzzy logic control systems. Concepts of Artificial Neural Networks: Basic Models and Learning rules of ANN's. Single layer perceptron networks – Feedback networks – Supervised and unsupervised learning approaches – Neural Networks in Control Systems. Basics of Genetic Algorithms: Evolution of Genetic Algorithm Applications. Integration of Fuzzy and Neural Systems: Neural Realization of Basic fuzzy logic operations – Neural Network based fuzzy logic inference – Neural Network based Fuzzy Modelling – Types of Neural Fuzzy Controllers. Fuzzy logic based Neural Network Models: Fuzzy Neurons – Type I, Type II, Type III – Fuzzification of Neural Network Models – Fuzzy Perceptron and Fuzzy classification with back propagation network Neural Networks with fuzzy training – Fuzzy Neural clustering.
**TEXTS:**
1. Jyh Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, *Neuro-Fuzzy and Soft Computing: AComputational Approach to Learning and Machine*, Prentice Hall. 1997
2. Chin –Teng Lin and C.S. George Lee, *Neural Fuzzy Systems" – A neuro fuzzy synergism toIntelligent systems*, Prentice Hall International. 1996
3. Yanqing Zhang and Abraham Kandel, *Compensatory Genetic Fuzzy Neural Networks andTheir Applications*, World Scientific. 1998.
4. T. J. Ross, *Fuzzy Logic with Engineering Applications*, McGraw-Hill, Inc. 1995

**EC530 Microcontroller for Embedded System 3-0-0-6**
ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families. Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions. Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions. Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops. Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.
**TEXTS:**
1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.
**REFERENCES:**
1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

**EC531 Embedded Computing 3-0-0-6**
System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. Tasks, Threads, Multi-Threading, Semaphore, Message Queue. GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools. Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with dataprocessing and display, OpenCV for machine vision, Audio signal processing. Sockets, ports, UDP, TCP/IP, client server model, socket programming,

802.11, Bluetooth, ZigBee, SSH, firewalls, network security. Application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

**TEXTS:**

1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals

**REFERENCES:**

1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens

**EC532 Hardware Software Codesign 3-0-0-6**

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis. Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure. Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems. Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment. Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification. System – level specification, design representation for system level synthesis, system level specification languages, Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

**TEXTS:**

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

**REFERENCES:**

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

**EC533 Embedded Networking 3-0-0-6**

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols - RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire. USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types – Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN. Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol. Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure. Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

**TEXTS:**

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

**REFERENCES:**

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - Bhaskar Krishnamachari , Cambridge press 2005.

**EC534 CPLD AND FPGA ARCHITECTURES AND APPLICATIONS 3-0-0-6**

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation. Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs. Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures. Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures. General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

**TEXTS:**

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

**REFERENCES:**

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

**EC 535 Semiconductor IC Technology 3-0-0 6**

Historical perspective, processing overview, crystal growth, wafer fabrication and basic properties of Silicon Wafers, Clean Rooms, Wafer Cleaning, Epitaxy, Thermal Oxidation of Silicon, Lithography, Wet and Dry Etching, Thin film deposition, Diffusion, Ion Implantation, Metallization, Process Integration: Passive components, Bipolar Technology, MOSFET Technology, MESFET Technology, MEMS Technology, IC Manufacturing: Electrical Testing, Packaging, Yield, Future trends and Challenges: Challenges for integration, system on chip.

**Texts:**

1. G. S. May and S. M. Sze, *Fundamentals of Semiconductor Fabrication*, Wiley India, 2004.
2. J. D. Plummer, M. D. Deal and P. B. Griffin, *Silicon VLSI Technology,Fundamentals, Practice and Modeling*, Pearson education, 2000.
3. S. M. Sze, *VLSI Technology*, 2nd Edn., TMH, 2004.
4. S. M. Sze, *Semiconductor Devices: Physics and Technology*, 2nd Edn., Wiley India, 2011.
5. W. R. Runyan and K. E. Bean, *Semiconductor Integrated CircuitProcessing Technology*, Addison Wesley Publishing Company, 1990.
6. S. A. Campbell, *The Science and Engineering of MicroelectronicFabrication*, Oxford University Press, 1996.
7. M. J. Madou, *Fundamentals of Microfabrication*, 2nd Edition, CRC Press, 2011.

**EC 536 VLSI System Design 3-0-0 6**

Basics of system hardware design: Hierarchical design using top-down and bottom-up methodology, System partitioning techniques, interfacing between system components, Handling multiple clock domains, Synchronous and asynchronous design styles; Design of finite state machines: state assignment strategies; The Processor: Data path and Control, Enhancing performance with Pipelining, exploiting of Memory hierarchy.

**Texts / References:**

1. G. De. Micheli, Synthesis and Optimisation of Digital Circuits, Tata McGraw-Hill, 2004.
2. D. A. Patterson and J. L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, 2nd Edition, Morgan Kaufmann Publishers, Inc, 1998.
3. J. Rabaey, Digital Integrated Circuits, A Design Perspective, 2nd Edition, Pearson Education, 2003.
4. H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, 2nd Edition, Eight Indian Reprint, Pearson Education, 2002.
5. C. Mead and L. Conway, Introduction to VLSI Systems, Addison Wesley, 1979.

**EC 537 Linear Algebra and Optimization 3-0-0 6**

Linear Algebra - vector spaces, linear independence, bases and dimension, linear maps and matrices, eigenvalues, invariant subspaces, inner products, norms, orthonormal bases, spectral theorem, isometries, polar

and singular value decomposition, operators on real and complex vector spaces, characteristic polynomial, minimal polynomial; optimization - sequences and limits, derivative matrix, level sets and gradients, Taylor series; unconstrained optimization - necessary and sufficient conditions for optima, convex sets, convex functions, optima of convex functions, steepest descent, Newton and quasi Newton methods, conjugate direction methods; constrained optimization - linear and non-linear constraints, equality and inequality constraints, optimality conditions, constrained convex optimization, projected gradient methods, penalty methods.

**Texts:**

1. S. Axler, *Linear Algebra Done Right*, 2nd Edn., Springer, 1997.
2. E. K. P. Chong and S. H. Zak, *An Introduction to Optimization*, 2nd Edn., Wiley India Pvt. Ltd., 2010.
3. G. Strang, *Linear Algebra and Its Applications*, Nelson Engineering, 2007.
4. D. C. Lay, *Linear Algebra and Its Applications*, 3rd Edition, Pearson, 2002.
5. D. G. Luenberger and Y. Ye, *Linear and Nonlinear Programming*, 3rd Edn., Springer, 2010.

**EC 538 Signal Processing Algorithms and Architectures3-0-0 6**

Orthogonal transforms: DFT, DCT and Haar; Properties of DFT;Computation of DFT: FFT and structures, Decimation in time,Decimation in frequency; Linear convolution using DFT; Digital filterstructures: Basic FIR/IIR filter structures, FIR/IIR Cascaded latticestructures, Parallel allpass realization of IIR transfer functions, Sinecosinegenerator; Computational complexity of filter structures;Multirate signal processing: Basic structures for sampling rateconversion, Decimators and Interpolators; Multistage design ofinterpolators and decimators; Polyphase decomposition and FIRstructures; Computationally efficient sampling rate converters;Arbitrary sampling rate converters based on interpolation algorithms:Lagrange interpolation, Spline interpolation; Quadrature mirror filterbanks; Conditions for perfect reconstruction; Applications in subbandcoding; Digital Signal Processors introduction: Computationalcharacteristics of DSP algorithms and applications; Techniques forenhancing computational throughput: Harvard architecture,parallelism, pipelining, dedicated multiplier, split ALU and barrelshifter; TMS320C64xx architecture: CPU data paths and control,general purpose register files, register file cross paths, memory loadand store paths, data address paths, parallel operations, resourceconstraints.

**Texts:**

1. R. Chassaing and D. Reay, *Digital signal processing and applicationswith TMS320C6713 and TMS320C6416*, Wiley, 2008.
2. S. K. Mitra, *Digital Signal Processing: A Computer Based Approach*,3rd Edn., TMH, 2008.
3. J. G. Proakis and D. G. Manolakis, *Digital Signal Processing:Principles, Algorithms and Applications*, Pearson Prentice Hall, 2007.

**EC 539 Optimal and Adaptive Signal Processing 3-0-0 6**

Review: Hilbert space of random variables; response of linear systemsto wide-sense stationary inputs, spectral factorization theorem andinnovation processes, autoregressive moving average processes; Linearminimum mean-square error (LMMSE) estimation: minimum mean squareerror(MMSE) estimation of jointly Gaussian random variables,LMMSE, orthogonality principle and Wiener Hoff equation; FIR Wienerfilters, linear prediction-forward and backward predictions, Levinson-Durbin Algorithm and lattice filter; IIR Wiener filters: non-causalWiener filter, innovation and and causal Wiener filter; Kalman filters:Gauss-Markov state variable models; innovation and Kalmanrecursion, steady-state behaviour of Kalman filters; Adaptive filters:steepest descent solution of FIR Wiener filter, LMS algorithm convergence,steady-state behaviour and practical considerations, RLSalgorithm- method of least-squares, recursive solution and square rootalgorithms, application of adaptive filters-equalization and noisecancellation. Spectral Estimation: Smoothed and windowed periodograms, minimum variance, maximum entropy and parametricmethods for spectral estimation, frequency estimation.

**Texts:**

1. M. H. Hayes, *Statistical Digital Signal Processing and Modeling*, JohnWiley & Sons, Inc., 2002.
2. S. Haykin, *Adaptive Filter Theory*, Prentice Hall, 2001.
3. D.G. Manolakis, V.K. Ingle and S.M. Kogon, *Statistical and AdaptiveSignal Processing*, McGraw Hill, 2000.
4. S. J. Orfanidis, *Optimum Signal Processing*, 2nd Edition, 2007republication of the 1988 McGraw-Hill edition.
5. S. M. Kay, *Fundamentals of Statistical Signal Processing: EstimationTheory*, Prentice Hall, 1993.
6. B. Widrow and S. D. Stearns, *Adaptive Signal Processing*, PrenticeHall, 1985.

**EC 540 Detection and Estimation Theory 3-0-0 6**

Review of random process, problem formulation and objective of signal detection and signal parameter estimation; Hypothesis testing:Neyman-Pearson, minimax, and Bayesian detection criteria;Randomized decision; Compound hypothesis testing; Locally anduniversally most powerful tests, generalized likelihood-ratio test;Chernoff bound, asymptotic relative efficiency; Sequential detection;Nonparametric detection, sign test, rank test. Parameter estimation:sufficient statistics, minimum statistics, complete statistics; Minimumvariance unbiased estimation, Fisher information matrix, Cramer-Raobound, Bhattacharya bound; Linear models; Best linear unbiasedestimation; Maximum likelihood estimation, invariance principle;Estimation efficiency; Least squares, weighted least squares; Bayesianestimation: philosophy, nuisance parameters, risk functions,minimum mean square error estimation, maximum a posterioriestimation.

**Texts:**

1. H. V. Poor, *An Introduction to Signal Detection and Estimation*, 2ndedition, Springer, 1994.
2. S. M. Kay, *Fundamentals of Statistical Signal Processing: Detection Theory*, Prentice Hall PTR, 1998.
3. S. M. Kay, *Fundamentals of Statistical Signal Processing: EstimationTheory*, Prentice Hall PTR, 1993.
4. H. L. Van Trees, *Detection, Estimation and Modulation Theory, Part I*,John Wiley, 1968.
5. D. L. Melsa and J. L. Cohn, *Detection and Estimation Theory*, McGrawHill, 1978.
6. L. L. Scharf, *Statistical Signal Processing: Detection, Estimation, andTime Series Analysis*, Addison-Wesley, 1990.
7. V. K. Rohatgi and A. K. M. E. Saleh, *An Introduction to Probability andStatistics*, 2nd edition, Wiley, 2000.

EC 541 **ASIC DESIGN AND MODELING 3-0-0-6**

Introduction to ASIC, Modeling combinational and sequential circuits, Design entry by verilog / VHDL /FSM / SYSTEM C, Hardware modeling with Verilog / VHDL, different verilog /VHDL constructs, and Logic Synthesis. ASIC construction, Simulation ,Verification of complex logic design model, Verification issues like verification plan, verification methodology, timing verification, Hardware design verification, Software design verification ,verification strategy for ASIC bus functional models, verification Automation, physical verification, Layout planning and verifications ,ASIC design flow and HDL based ASIC design flow, EDA tools for ASIC design, Mixed signal design , Introduction to VLSI physical design, floor planning , placement and routing parameter extraction , static timing analysis , current analysis , clock tree synthesis , power grid analysis , clock skew analysis and post layout synthesis , Data structure for graph models, , different tools for the PAR, Design rule and electric rule checking, LVS , Wire length / load estimator, stick diagrams by using CMOS for various combination ckt and Different timing parameters for Asics. Test specification , need for testability, Boundary Scan Test , Faults , Fault simulation , Automatic Test pattern Generation , SCAN test , Built in Self test ,Gate level simulation and IC verification. Tools used for front to back end chip design.

**Texts:**

1. Wayne Wolf, "Modern VLSI Design " by Pearson Education Asia, 2000.
2. Michael Smith ,"Application Specific Integrated Circuits –" by Pearson Education Asia, 2007.
3. Geiger , Allen Strader,"VLSI Design Techniques for Analog and Digital circuits " McGraw HILL, 1999.
4. Neil Weste ," Principles of CMOS VLSI Design "by Pearson Education Asia, 2007.

**EC 542 MACHINE INTELLIGENCE 3-0-0-6**

Introduction, Soft Computing intelligence, comparison with conventional Artifical Intelligence, soft computing characteristics, Fuzzy sets, Fuzzy rules and Fuzzy inference systems, Different fuzzy Models : Mamdani, Sugeno, Tsu Kamoto, Fuzzy modeling, Least squares methods for system identification, Derivative based optimization. Neural networks, Adaptive networks, Supervised learning Neural networks, Perceptron, Backpropagation Multilayer perceptron , Radial basis function networks, Learning from reinforcement, Dynamic programming, Competitive learning, Kohonen's self organizing networks, Principle component networks, LVQ, Hopfield networks. Adaptive Neuro-Fuzzy interface systems, Advanced Neuro-Fuzzy modeling, Data clustering algorithms, Neuro-Fuzzy control, Fuzzy filtered neural network, Genetic algorithms in game playing.

**Texts:**

1. S. R. Jang, C.T. Sun, E. Mizutani,' Neuro-Fuzzy and Soft Computing', Pearson Education, ISBN 81-297-0324-6, 1989.
2. B. Kosko, 'Neural Networks and Fuzzy Systems : a dynamical systems approach' Prentice Hall Publication, 1993.
3. Simon Haykin, ' Neural Networks : comprehensive foundation', Prentice Hall, ISBN-10: 0132733501, 1987.
4. Jacek M. Zurada , 'Introduction to Artifical Neural Systems', Jaico publications, 2000.

**EC 543 Reconfigurable Computing 3-0-0 6**

Computing requirements, Area, Technology scaling, Instructions, Custom Computing Machine, Overview, Comparison of Computing Machines. Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement, Routing; Computing Elements, LUT's, LUT Mapping, ALU and CLB's, Retiming, Fine-grained & Coarse-grained structures; Multicontext; Comparison of different architectures viz. PDSPs, RALU, VLIW, Vector Processors, Memories, Arrays for fast computations, CPLDs, FPGAs, Multicontext, Partial Reconfigurable Devices; TSFPGA, DPGA, Mattrix; Best suitable approach for RD; Case study. Control Logic, Binding Time and Programming Styles, Overheads, Data Density, Data BW, Function density, Function diversity, Interconnect methods, Best suitable methods for RD; Contexts, Context switching; Area calculations for PE; Efficiency, ISP, Hot Reconfiguration; Case study. Architectures for existing multi FPGA systems, Compilation Techniques for mapping applications described in a HDL to reconfigurable hardware, Study of existing reconfigurable computing systems to identify existing system limitations and to highlight opportunities for research; Software challenges in System on chip; Testability challenges; Case studies. Modelling , Temporal portioning algorithms, Online temporal placement, Device space management, Direct communication, Third party communication, Bus based communication, Ckt switching, Network on chip, Dynamic network on chip, Partial reconfigurable design.

**Texts:**

1. IEEE Journal papers on Reconfigurable Architectures.
2. "High Performance Computing Architectures" (HPCA) Society papers.
3. Christophe Bobda, "Introduction to Reconfigurable Computing", Springer Publication, 2009.
4. Maya Gokhale, Paul Ghaham, "Reconfigurable Computing", Springer Publication, 2011.

**EC 544 Memory Technologies 3-0-0 6**

Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOl, Advanced SRAM Architectures, Application Specific SRAMs; DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM, High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing. General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.

**Texts:**

1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice- Hall of India Private Limited, New Delhi, 1997.
2. Memories", Springer Publication.
3. Wen C. Lin, "Handbook of Digital System Design", CRC Press.

**EC 545 VLSI EDA TOOLS 3-0-0-6**

ASIC design flow, various design entries, IP cores, cross compilers, cell design, stick diagrams, synthesis, place and route, floor planning, power estimation, static timing analysis, dynamic timing analysis, antenna rules, design rule check, electric rule check, schematic rule check, Clock domain crossing check, layout verses schematic, layout techniques, verification, manufacturing tests. Xilinx ISE, Actel libero, Active HDL, Sinplify pro, Leonardo spectrum, Quartus, Boole Dozer, Model Simdesign entries, various simulation, synthesis, place and route, timing verification. Cadence, IC station – design entries, simulations, various tools in the suit, GDS files. Microwind, Spice, Magic – layout techniques, simulations, DRCs, , tools available in the suit.

**Texts:**

1. Michael Smith, "Application Specefic Integrated Circuits", Pearson Education Asia, 2000.
2. Reference manuals of the respective tools.

**EC 546 Fault Tolerance System Design 3-0-0-6**

Modeling: Basic Concept, Functional modeling at the logic level, Functional models at the register level, Structural models, Level of modeling. Type of simulation, unknown logic value, compiled simulation, Event-driven simulation and Hazard Detection. Logical fault models, Fault detection and redundancy, Fault equivalence and fault location, Fault Dominance, Single stuck-fault models, multiple stuck fault model, stuck

RTL variables, Fault variables. Testing for Single Stuck fault and Bridging fault. General fault simulation techniques, Serial Fault simulation, Parallel fault simulation, Deductive fault simulation, Concurrent fault simulation, Fault simulation for combinational circuits, Fault sampling, Statistical fault analysis. General aspects of compression techniques, ones- count compression, transition – count compression, Parity – check compression, Syndrome testing and Signature Analysis Basic concepts , Multiple – Bit Errors , Checking circuits and self checking , self – checking checkers , Parity – check function , totally self-checking m/n code checkers , totally self checking equality checkers , Self-checking Berger code checkers and self checking combinational circuits.Built In Self Test, Self testing circuits for systems, memory & processor testing, PLA testing, Automatic test pattern generation and Boundary Scan Testing JTAG

**Texts:**

1. M.Abramovici, M.A. Breuer, A.D. Friedman, "Digital systems testing and testable design", Jaico Publishing House, 2009.
2. Diraj K. Pradhan, "Fault Tolerant Computer System Design", Prentice Hall, 2000.

**EC 547 Biomedical Signals & Systems 3-0-0-6**

Introduction to Biomedical Signals,Nature of Biomedical Signals, Examples of Biomedical Signals – EMG, ECG, EEG, ERPs,PCG,VMG, VAG, Objectives of Biomedical Signal Analysis, Difficulties in Biomedical Signal Analysis, Concurrent, Coupled, and Correlated Processes- Illustration of the Problem with Case-Studies. Filtering for Removal of Artifacts- Illustration of the Problem with Case-Studies,Time-Domain Filters, Frequency-Domain Filters, Optimal Filtering, The Wiener Filter, Adaptive Filters for Removal of Interference, Selecting an Appropriate Filter Application: Removal of Artifacts in the ECG, Event Detection, Detection of Events and Waves, Correlation Analysis of EEG channels, Cross-spectral Techniques. The Matched Filter, Detection of the P Wave, Homomorphic Filtering, Application- ECG Rhythm Analysis, Identification of Heart Sounds, Waveshape and waveform Complexity, Analysis of Event-related Potentials, Morphological Analysis of ECG Waves, Envelope Extraction and Analysis of Activity, Application- Normal and Ectopic ECG Beats, Analysis of Exercise ECG. Frequency-domain Characterization The Fourier Spectrum, Estimation of the Power Spectral Density Function, Measures Derived form PSDs. Modeling Biomedical Systems, Point Processes Parametric System Modeling Autoregressive of Allpole Modeling, Pole-Zero Modeling, Electromechanical Models of Signal Generation, Application- Heart-rate Variability, Spectral Modeling and Analysis of PCG. Analysis of Nonstationary Signals, Time-Variant Systems, Fixed Segmentation, Adaptive Segmentation, Use of Adaptive Filters for Segmentation, Application- Adaptive Segmentation of EEG Signals, Adaptive Segmentation of PCG Signals. Pattern Classification and Diagnostic Decision , Pattern Classification, Supervised Pattern Classification, Unsupervised Pattern Classification, Probabilistic Models and Statistical Decision , Logistic regression Analysis The Training and Test Steps, Neural Networks, Measures of Diagnostic Accuracy and Cost, Reliability of Classifier and Decisions

**Texts:**

1. R. M. Rangayyan "Biomedical Signal Analysis- A case study approach", Wiley Publications, 2006.
2. Eugene N Bruce "Biomedical signal processing and signal modeling", Wiley publications, 2007.

**EC 548 Advanced Digital System Design 3-0-0-6**

Digital System Design aspects for RISC and CISC CPU architectures. Control and Data path units of Processor. Practical design aspects for high frequency digital design such as clock skew and synchronous / asynchronous input signal handling. Hazard analysis, fault tree analysis. Estimation of digital system reliability. System integrity. Design of digital system for network applications such as ATM switch design, ATM packet generator, ATM packet decoder. Hardware testing and design for testability: Testing combinational and sequential logic, scan testing, boundary scan and BIST. VHDL models for memories and buses such as SRAM memory, 486 bus model and memory interfacing with microprocessor bus. Floating point arithmetic operations such as multiplications and others. Digital system design for asynchronous serial data transfer.

**Texts/References:**

1. John F. Wakerly,"Digital Design principles and practices, PHI publications, 2003.
2. Charles H. Roth, "Digital system design using VHDL", Thomson Publication, 2001.
3. Balabanian,"Digital logic design principles",Wiley publication, 1999.
**4.** Stephen Brown, "Fundamentals of digital logic", TMH publication, 2010.

**EC 549 Embedded Automotive Systems 3-0-0-6**

Current trends in Automobiles, open loop and closed loop systems - components for electronic engine management system. Electro magnetic interference suppression. Electromagnetic compatibility, Electronic

dashboard instruments, onboard diagnostic system , security and warming system. Electronic management of chassis systems. Vehicle motion control. Sensors and actuators, and their interfacing. Basic sensor arrangement, types of sensors such as- oxygen sensors, crank angle position sensors- Fuel metering/ vehicle speed sensors and destination sensors, Attitude sensor, Flow sensor, exhaust temperature, air mass flow sensors. Throttle position sensor, solenoids, stepper motors, relays. Electronic ignition systems. Types of solid state ignition systems and their principle of operation. Digital engine control system. Open loop and closed loop control system, Engine cranking and warm up control. Acceleration enrichment. Deceleration learning and ideal speed control, Distributor less ignition – Integrated engine control system, Exhaust emission control engineering. Automotive Embedded systems. PIC, Freescale microcontroller based system. Recent advances like GLS, GPSS, GMS. Multiprocessor communication using CAN bus. Case study- cruise control of car. Artificial Intelligence and engine management.

**Texts:**

1. William B. Riddens, "Understanding Automotive Electronics", 5th Edition, Butterworth Hennimann Woburn, 1998.
2. Young A.P. & Griffiths, " Automotive Electrical Equipment" , ELBS & New Press- 1999.
3. Tom Weather Jr. & Cland c. Ilunter, " Automotive computers and control system" Prentice Hall Inc., New Jersey, 1998.
4. Crouse W.H., " Automobile Electrical Equipment" , Mc Graw Hill Co. Inc., New York ,1995.
5. Bechhold, " Understanding Automotive Electronic", SAE,1998.
6. Robert Bosch," Automotive Hand Book", SAE (5TH Edition),2000.

**EC 550 System-on-Chip (SoC) 3-0-0-6**

IC Technology, Economics, CMOS Technology overview, Power consumption, Hierarchical design, Design Abstraction, EDA tools. MOSFET model, parasitics, latch up, advanced transistor structures; Wire parasitics; Design rules, Scalable design rules, process parameters; stick diagrams, Layout design tools; Layout synthesis, layout analysis. CMOS gate delays, transmission time, speed power product, low power gates; Delay by RC trees, cross talk, RLC delay, cell based layout, Logic & interconnect design, delay modeling, wire sizing; Power optimization, Switch logic networks. Pipelining, Data paths, Adders, ALUs, Multipliers, High density memories; Metastability, Multiphase clocking; Power optimization, Design validation, Sequential testing; Architecture for low power. Floor planning methods, global routing, switch box routing, clock distribution; off chip connections, packages, I/O architectures, pad design. Complete chip design including architecture, logic and layout for Kitchen timer chip OR Microwave oven chip.

**Texts**

1. Wayne Wolf, "Modern VLSI Design", Pearson Education, 1998.
2. Kamaran Eshraghian, "Principles of CMOS VLSI Design", Pearson Education, 2007
3. Rabey, Chandrakasan, "Digital IC Design", Preason Publication, 2009.

**EC 551 Software Defined Radio 3-0-0-6**

SDR concepts & history, Benefits of SDR, SDR Forum, Ideal SDR architecture, SDR Based End-to-End Communication, Worldwide frequency band plans, Aim and requirements of the SCA, Architecture Overview, Functional View, Networking Overview, Core Framework, Real Time Operating Systems, Common Object Request Broker Architecture (CORBA), SCA and JTRS compliance, Radio Frequency design, Baseband Signal Processing, Radios with intelligence, Smart antennas, Adaptive techniques, Phased array antennas, Applying SDR principles to antenna systems, Smart antenna architectures, Low Cost SDR Platform, Requirements and system architecture, Convergence between military and commercial systems, The Future For Software Defined Radio

**Texts/References:**

1. Dillinger, Madani, Alonistioti (Eds.): Software Defined Radio, Architectures, Systems and Functions, Wiley 2003
2. Reed: Software Radio, Pearson, 1997.
3. Software Defined Radio for 3G, 2002, by Paul Burns.
4. 4.Tafazolli (Ed.): Technologies for the Wireless Future, Wiley 2005.
5. Bard, Kovarik: Software Defined Radio, The Software Communications Architecture, Wiley, 2007.

**552 EC SMART ANTENNAS 3-0-0-6**

Antenna gain, Phased array antenna, power pattern, beam steering, degree of freedom, optimal antenna, adaptive antennas, smart antenna - key benefits of smart antenna technology, wide band smart antennas, Digital radio receiver techniques and software radio for smart antennas. Signal model conventional beamformer, null steering beamformer, optimal beamformer, Optimization using reference signal, beam space processing. Sample matrix inversion algorithm, unconstrained LMS algorithm, normalized LMS algorithm, Constrained LMS algorithm,

Perturbation algorithms, Neural network approach, Adaptive beam space processing, Implementation issues. Tapped delay line structure, Partitioned realization, Derivative constrained processor, Digital beam forming, Broad band processing using DFT method. Spectral estimation methods, linear prediction method, Maximum entropy method, Maximum likelihood method, Eigen structure methods, Music algorithm – root music and cyclic music algorithm, the ESPRIT algorithm. Spatial diversity selection combiner, switched diversity combiner, equal gain combiner, maximum ratio combiner, optical combiner.

**TEXTS:**


1. Lal Chand Godara, "Smart Antennas" CRC press, 2004.
2. Joseph C Liberti.Jr and Theodore S Rappaport, "Smart Antennas for Wireless Communication: IS-95 and Third Generation CDMA Applications", Prentice Hall 1999.
3. Balanis, "Antennas", John Wiley and Sons, 2005.


**EC553 Filters Design 3-0-0-6**

Signals, Noise and Information, Signal Processing Methods, Transform-Based Signal Processing, Source-Filter Model-Based Signal Processing. Bayesian Statistical Model-Based Signal Processing. Different classes of noises and distortion, Linear prediction models, forward and backward models, Eigenvalue and PCA, power spectrum analysis. Impulse noise modelling, detection and removal. Impulse noise using linear prediction models.

TEXTS:


1. S.V. Vaseghi, Advance signal processing and noise reduction, Wiley, 2008.